



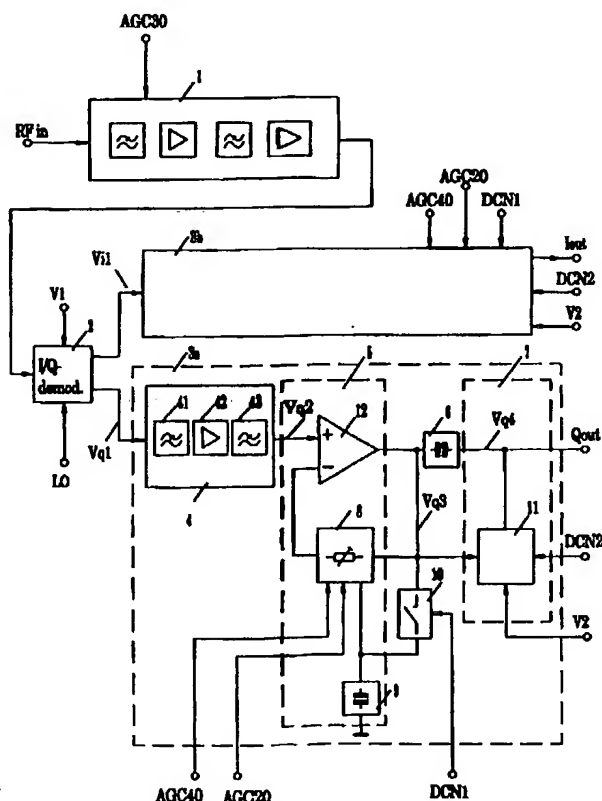
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<p>(21) International Application Number: PCT/FI97/00073</p> <p>(22) International Filing Date: 6 February 1997 (06.02.97)</p> <p>(30) Priority Data: 960577 8 February 1996 (08.02.96) FI</p> <p>(71) Applicant (for all designated States except US): NOKIA MOBILE PHONES LTD. [FI/FI]; P.O. Box 86, FIN-24101 Salo (FI).</p> <p>(72) Inventor; and (75) Inventor/Applicant (for US only): VÄISÄNEN, Risto [FI/FI]; Vähäsillankatu 10 B 5, FIN-24100 Salo (FI).</p> <p>(74) Agent: BERGGREN OY AB; P.O. Box 16, FIN-00101 Helsinki (FI).</p>		<p>(81) Designated States: AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).</p> <p><b>Published</b></p> <p><i>With international search report.</i></p> <p><i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i></p>

**(54) Title: METHOD AND CIRCUIT ARRANGEMENT FOR PROCESSING A RECEIVED SIGNAL**

**(57) Abstract**

The invention relates to a method and a circuit arrangement for processing a received signal in a direct conversion receiver. The invention can be preferably applied in mobile stations which are used in digital, time-division cellular systems. A direct voltage component of a signal which has been received and converted to a baseband is separated by the first separating means (6) of direct voltage in a signal line and additionally, the direct voltage components of both the signal preceding the separating means and the signal following the separating means are controlled by control signals (DCN1, DCN2). Thus the baseband signal line (4, 5) preceding the first separating means (6) can be implemented essentially as direct voltage coupled. The control circuit (5) of signal strength preceding said first separating means (6) comprises preferably a second separating means (9) for separating the direct voltage component occurring in the control circuit (5) from the constant potential of the circuit arrangement such as the ground level. Then one of said control signals (DCN1) has been preferably arranged to control the charge state of the second separating means (9). The baseband signal following the separating means is converted preferably into a digital form for further processing of the signal.



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## Method and circuit arrangement for processing a received signal

The invention relates to a method and a circuit arrangement for receiving a radio frequency signal. The invention can be applied preferably in receivers of digital, time-division data transfer systems, such as in mobile stations.

In a direct conversion receiver, that is in a zero intermediate frequency receiver, a radio frequency signal is converted directly to a baseband without there being intermediate frequency. Since intermediate frequency stages are not needed, only a few components are needed in a receiver, which makes it a preferable solution for use in various applications. In mobile stations, direct conversion receivers are, however, used rarely. On one hand, this is due to the fact that prior known methods are almost impossible to implement in practice in industrial manufacturing or on the other hand, in presented solutions the unique features of digital mobile phone systems have not been taken into consideration. The most important problem in the implementation of a direct conversion receiver is the control of offset voltages. By an offset voltage one means voltage which has become summed up in a signal, essentially direct voltage which is not included in a received useful signal.

Fig. 1 shows a prior known block diagram of a transmitter-receiver of a mobile station and in this block diagram, the receiver is a direct conversion receiver. In it, an RF signal received by an antenna 138 is conducted via a duplex filter 102 to a pre-amplifier 104. The purpose of the duplex filter is to permit the use of the same antenna both in transmitting and receiving. Instead of a duplex filter, also a synchronous antenna changeover switch can be used in a time-division system. An RF signal which is received from an amplifier 104 is low-pass filtered 106 and demodulated in an I/Q demodulator 108 into an in-phase signal 108a and into a quadrature signal 108b. A local oscillator signal 114b which is needed in demodulation is received from a synthesizer 114. In block 110, removal of direct voltage and automatic gain control (AGC) are carried out. Block 110 is controlled by a processing block 116 which may contain, for example, a micro-processor. Automatic gain control is regulated by a signal 110a and removal of the offset voltage is regulated by a signal 110b. Signals

received from block 110 are converted into digital signals in block 112 from which the signals are further led to digital signal processing circuits in the processing block 116.

- 5 The transmitter unit comprises an I/Q modulator 128 which forms from an in-phase signal 128a and from a quadrature signal 128b, a carrier-frequency signal which is low-pass filtered and/or high-pass filtered by a filter 130. The carrier-frequency signal is amplified by an RF amplifier 132 and the amplified signal is transferred via a duplex filter 102 to an antenna  
10 138. A power control unit 134 of the transmitter controls the amplification of the RF amplifier 132 on the basis of the measured output power 136 and of the control 134a received from the processor.

Fig. 1 also shows, attached to the processing unit, the memory unit 126  
15 and user interface means which comprise a display 118, a keyboard 120, a microphone 122 and an earpiece 124.

Practical solutions for implementation of a direct conversion receiver have been described more closely, for example, in the following publications:

20

- [1] Microwave Engineering Europe, January 1993, pages 59 ... 63,
- [2] Microwave Engineering Europe, May 1993, pages 53 ... 59 and
- [3] patent application EP 0 594 894 A1.

- 25 The solution for a receiver presented in the reference [1] is based on direct voltage coupled baseband parts and in them the DC offset voltage compensations are attained via extremely complicated control systems which contain D/A converters, A/D converters, digital filters and predicting control algorithms. Various correction values are stored into memories, for  
30 example, for different channels and for AGC adjustments.

When a DC-coupled baseband part is used, great fluctuations in direct voltage can create a problem. Fluctuations in a direct voltage component of a signal may be due to, for example, temperature changes in which case  
35 they are typically slow or, for example, due to variations in frequency or level of a local oscillator signal in which case the fluctuations in direct voltage are rapid. Also a received signal may contain, due to modulation, a direct voltage component which cannot be removed, which makes the

determination of the real offset voltage extremely difficult and complicated. When the above mentioned complicated solutions for control of the offset voltage are used, the manufacturing costs of the device become so great that the advantages of the direct conversion receiver are lost.

5

The advantage of the AC-coupled baseband parts is that slow fluctuations in offset voltage are dissipated and the total amount of the offset voltage can be reduced. The disadvantage is, however, that there may be charges which remain in the separating capacitors of the direct voltage and which  
10 discharge slowly.

Fig. 2 shows a prior known solution for reducing the offset voltage of a signal. In a circuit according to Fig. 2, a baseband signal  $V_{in}$  is conducted to an amplifier 21, the output P21 of which has been conducted via a  
15 capacitor C21 to the input P22 of an amplifier 22. In the place of the amplifier 22, it is also possible to have, for example, an analog/digital converter. A reference voltage has been conducted to the input of the amplifier 22 via a resistor R21. Prior to the start of the receiving, a short control pulse DCN connects a switch 23 to an on-state and then the output  
20 terminal of the capacitor C21 becomes set at a reference voltage  $V_{ref}$  and at the point P22 if there is any offset voltage, it is dissipated. If, at the moment of the removal of the offset voltage, there is, for example, a positive baseband useful signal in addition to the offset voltage on the signal path, the DCN control pulse removes the offset voltage occurring at  
25 the point P22 but, as the DCN control pulse ends, a negative offset voltage is generated at the point P22. In this situation the offset voltage is thus not dissipated but the operation of the removing circuit of the offset voltage results in a new offset voltage which falls slowly towards the reference voltage  $V_{ref}$ . The offset voltage caused by the removing circuit of the  
30 offset voltage depends on the extent of the instantaneous value of the baseband signal occurring in the capacitor C21 at the moment when the DCN control pulse ends.

In order to circumvent the new offset voltage resulting from the removing  
35 circuit of the offset voltage, in the solution described above, the zeroing of the offset voltage should be performed at such an instant when the received signal is essentially noise, which means in practice before the onset of the signal reception. In many time-division systems for mobile

communications, such as GSM (Global System for Mobile Communications) and PCN (Personal Communications Network) systems, the power transmitted by the base station is not disconnected before the start of a new time interval. Thus there are baseband signals present in a receiver also before the start of the actual moment of reception, that is during the time when the offset voltage should be removed. This is why the earlier mentioned solution for reducing the offset voltage is not applicable in the above mentioned systems.

- 10 The aim of the invention is to devise a simple solution for implementation of a direct conversion receiver so that the above mentioned problems connected to the solutions according to prior art can be avoided.

One idea of the invention is that the direct voltage component of the signal which has been received and converted to a baseband is separated by the first separating means of direct voltage in a signal line and, in addition, the direct voltage components of both the signal preceding the separating means and of the signal following the separating means are controlled by control signals. Thus the baseband signal line which precedes the first separating means can be implemented essentially as direct voltage coupled. The control circuit of signal strength which precedes the above mentioned first separating means comprises preferably a second separating means for separating the direct voltage component occurring in the control circuit from constant potential of the circuit arrangement such as the ground level. Then one of the above mentioned control signals has been preferably arranged to control the charge state of the second separating means. The baseband signal following the separating means is preferably converted to a digital form for further processing of the signal.

- 30 A method according to the invention is characterized by the fact that the direct voltage component of the first signal preceding the above mentioned first separating means of direct voltage is controlled on the basis of the first control signal and the direct voltage component of the second signal following the above mentioned first separating means of direct voltage is controlled on the basis of the second control signal, which second control signal may be identical to said first control signal.

It is characteristic of a circuit arrangement according to the invention that the circuit arrangement comprises means for controlling the direct voltage component of a signal preceding the above mentioned separating means on the basis of the first control signal and means for controlling the direct voltage component of a signal following the separating means on the basis of the second control signal, which second control signal may be identical to the above mentioned first control signal. Preferable embodiments of the invention have been presented in the dependent claims.

10 The invention is described in the following in more detail by using the attached drawings in which

fig. 1 shows a block diagram of a prior known mobile station in which a direct conversion receiver has been used,

15

fig. 2 shows a prior art circuit arrangement for removing the offset voltage,

fig. 3 shows a flow diagram of a method according to the invention,

20

fig. 4 shows a circuit arrangement according to the invention for the implementation of a direct conversion receiver,

25 fig. 5 shows an implementation of a circuit arrangement according to the invention as a circuit diagram and

fig. 6 shows a solution according to the invention for reducing the offset voltage.

30 Figs. 1 and 2 were described above in the context of the description of the prior art. In the following, a method according to the invention is described briefly by using Fig. 3 and in more detail a circuit arrangement according to the invention and its operation by using Figs. 4 and 5. Finally, a solution according to the invention for reducing the offset voltage is described by referring to Fig. 6.

35

Fig. 3 shows a flow diagram of a method 300 according to the invention. In it, at first all gain controls are set to a state in which gain is the lowest

possible, block 301. After this, the local oscillator frequency of the frequency synthesizer is set at the channel frequency. After the frequency synthesizer has started to settle at the desired channel frequency, the gain control of the front of the RF is connected to the state in which it is going to be used during the time interval of reception, block 303. Thereafter, the direct voltage component of the first signal of the gain control part of the baseband frequency part is controlled by a control signal DCN1, block 304, and the direct voltage component of the second signal following the separating part of direct voltage is controlled by a control signal DCN2, block 305. Finally, prior to the onset of the time interval of reception, the controls DCN1 and DCN2 are removed and at the start of reception, a desired gain is chosen to the baseband frequency part by AGC controls of the baseband frequency part, block 306.

Fig. 4 shows a diagram depicting the principles of the circuit arrangement according to the invention. The parts presented in Fig. 4 correspond to blocks 104-112 of the transmitter/receiver part of the mobile station shown in Fig. 1. In the arrangement shown in Fig. 4, a radio frequency signal  $R_{Fin}$  received from an antenna is filtered and amplified in block 1 and demodulated to a baseband frequency in an I/Q demodulator 2. The RF front 1 of the receiver comprises RF amplification and RF filtering operations and the operation of automatic gain control AGC30.

The radio frequency signal is demodulated in an I/Q demodulator 2 which comprises phasing and power dividing elements, mixers and connection to the reference voltage  $V_I$ . The reference voltage may be positive, negative or zero depending on the ways the I/Q demodulator and the baseband frequency part are implemented. Demodulation is implemented by using a local oscillator signal  $LO$  which is fed to the demodulator. A quadrature signal  $V_{q1}$  and an in-phase signal  $V_{i1}$  which are received from the demodulator are conducted to baseband frequency parts 3a and 3b. The baseband frequency parts 3a, 3b contain pre-amplification and filtering parts (4) which further contain a passive low-pass filtering part 41 directly after the mixers of the I/Q demodulator before the first active stage, a pre-amplification part 42 after which the second low-pass filters 43 are placed.

After pre-amplification and filtering, the signals are conducted to gain control parts 5 which contain an amplification part 12, a feedback part 8



and a second separating means 9 of direct voltage of the feedback part in which there is preferably at least one capacitor. The settling speed of the direct voltages of the gain control parts 5 is controlled by a selector switch 10 which is controlled by a signal DCN1.

5 To the output of the gain control, the first separating means 6 of direct voltage has been connected which comprises preferably at least one capacitor. After the separating part 6 of direct voltages, a removing system 7 for the offset voltage is placed and a solution for its implementation has  
10 been presented later on. Removing of the offset voltage occurring in a signal following the second separating means is controlled by a signal DCN2. To the separating part of direct voltage, a reference voltage V2 of the A/D converter part is additionally fed which can also be identical to the reference voltage VI.

15 One difference between the invention and prior known solutions for receivers is that the entire baseband signal path from the reference voltage VI of the I/Q demodulator to the output of the AGC amplifiers 5 has been coupled to direct voltage and on the signal path there is only one DC  
20 separating part 6 in each branch after the AGC part. Via this arrangement, for example, the following advantages are achieved compared to other methods:

Offset voltages which are present, for different reasons, at the output of the  
25 I/Q demodulator need not be removed from the output of the I/Q demodulator, from the output of the baseband pre-amplifier or from the output of the AGC amplifier part but direct voltages can fluctuate freely. By an accelerating switch 10, the time constant of the feedback circuit is kept rapid during the time when direct voltages are settling. After the  
30 direct-voltage separating part 6 the direct voltage can be adjusted to be equal to the reference voltage V2 independent of the voltage at which the direct voltage operating point of the AGC amplifier part has settled. In this way, the advantages of the DC- and AC-coupled baseband parts have been combined and their disadvantages eliminated.

35 Digital control signals are used in the above described circuit arrangement according to Fig. 4 as follows:

- Initially, all the AGC controls are in a state where the gain is as low as possible. After the frequency synthesizer has started settling at the desired channel frequency, the gain control AGC30 of the front is connected to the state in which it is going to be used during the time interval of reception.
- 5 Thereafter, the time constant circuit of the gain control part of the baseband part is controlled to a fast state and the removing circuit 11 of the DC offset voltage to an active state by the controls DCN1 and DCN2. Prior to the start of the reception time interval, the controls DCN1 and DCN2 are removed. At the start of the reception, a desired gain is chosen to the
- 10 baseband part by the AGC controls AGC20, AGC40 of the baseband part. When strong antenna signals are received, the control DCN1 is not necessarily needed since the used gain of the baseband part is small and correspondingly, the offset voltages are low.
- 15 In Fig. 4, there are two AGC controls shown, AGC20 and AGC40, of the baseband part but there can be more or less of them depending, for example, on the dynamic range of the A/D converter and the means of implementation of baseband parts.
- 20 Fig. 5 shows an example of how the blocks 5, 10 and 6 from Fig. 4 can be implemented. In it, the gain of the amplification circuit is determined on the basis of feedback resistors R1, R3 and R7 and of resistors R2, R4, R5 and R6 which are connected to the ground from the feedback circuit as well as of capacitors C1 and C2. The capacitors C1 and C2 operate as
- 25 separators of direct voltage and thus there are two DC separating parts C1, R5 as well as C2, R6 at the feedback branch. By using two separate DC separating parts, the capacitance value of the capacitors used can be significantly reduced and the settling speed of direct voltages increased. The resistors R5 and R6 are intended to reduce the gain of the amplifier
- 30 when the acceleration circuit is in use. The switches can be, for example, CMOS switches.

- Fig. 6 shows a diagram depicting the principles of a circuit arrangement according to the invention for the implementation of the removing circuit
- 35 11 of the offset voltage. The circuit arrangement can be used, for example, in blocks 6 and 7 of the receiver shown in Fig. 4. In the arrangement shown in Fig. 6, the baseband signal  $V_{in}$  is conducted to the input of the amplifier 61 and the first signal  $s_{61}$  occurring at the output P61 of the

amplifier 61 has been conducted into two branches: via the capacitor C61 to the amplifier 62 and via the high-pass filter 64 to the summer 65. By using the summer, the high-pass filtered signal s63 is summed to the reference voltage Vref. The summing result, that is the second signal s62,  
5 is led to the switch 63 which is controlled to an on-state by a short control pulse DCN. In the terminals of the capacitor C61 there is during the entire DCN control pulse virtually the same baseband signal in which case there is hardly any charge created by the baseband signal in the capacitor. In that way no significant offset voltage is formed at the output when the DCN  
10 control pulse ends and the switch 63 is switched off.

In the solution according to the invention, the baseband signal passing through the signal line is not interrupted for the duration of the DCN control pulse but a high-pass filtered baseband signal occurs at the output  
15 of the capacitor during the DCN control pulse. The lower limiting frequency of the high-pass filter 64 is preferably higher than the lower limiting frequency of the signal line. Then the offset voltage occurring in the second signal is attenuated rapidly and, by connecting the second signal to the output of the separating means, also the offset voltage occurring in it  
20 can be rapidly reduced. The higher lower limiting frequency of the high-pass filter does not, however, have any effect on the band of the actual signal line except during the DCN control pulse.

By using the present invention it is possible to devise simply a direct  
25 conversion receiver which can be used in the construction of a mobile station. In mobile stations, the implementation of direct conversion receivers results in considerable cost savings since only one frequency synthesizer is necessary and there is no need for intermediate frequency parts or intermediate frequency filters. Also the RF shielding requirement  
30 decreases and a duplex filter is not necessary. Thus it is possible to construct a mobile station which is smaller in size and lighter in weight by lower costs. Furthermore, the current consumption of the mobile station can be reduced.

35 By using the solution according to the present invention for controlling the direct voltage components of a signal, the following additional advantages can be achieved compared to solutions according to prior art:

- digital signal processing is not necessary for correction of offset voltage
- since offset voltage can be reduced reliably from an analog signal, the dynamic range of analog/digital converters need not be increased because of the offset voltage,
- 5 - the operation of reducing the offset voltage does not cause even a momentary interruption of the baseband signal in a signal line,
- the solution according to the invention can be implemented by a small number of components which thus require little space and the additional manufacturing costs are very small,
- 10 - components which are needed in the circuit solution can be easily integrated to the connection of an A/D converter,
- by using the solution according to the invention, a small current consumption of the receiver is achieved,
- by using this solution, problems created by clock signals and other  
15 interfering signals of a stable frequency which impact on the frequency of the received channel can be removed, which lessens the need for shielding of the device.

20 A solution according to the invention is applied preferably in receivers of digital time-division mobile communication systems such as GSM and PCN systems, but the invention can be applied also in receivers of analog systems, for example, if the received analog signal is converted to a digital form for signal processing.

25 Some embodiments of the solution according to the invention have been presented above. Naturally the principle according to the invention can be modified within the frame of the scope of the claims, for example, by modification of the details of the implementation and the ranges of use. It should be noted that the presented circuit connections and component  
30 values have been described only as examples and they can be modified according to generally known design principles.

Claims

1. A method for processing a received signal when the received radio frequency signal is demodulated to a baseband, the strength of the baseband signal is controlled by a control circuit and direct voltage occurring in the baseband signal is separated by the first separating means (6, C1) of direct voltage in the signal line, after which the signal is A/D converted, **characterized** in that the direct voltage component of the first baseband signal preceding said first separating means of direct voltage is controlled (304) on the basis of the first control signal (DCN1) and the direct voltage component of the second baseband signal following said first separating means of direct voltage is controlled (305) on the basis of the second control signal (DCN2) which second control signal may be identical to the first control signal.
2. A method according to claim 1, **characterized** in that the signal which is demodulated to a baseband is conducted to said separating means essentially as direct voltage coupled.
3. A method according to claims 1 or 2, **characterized** in that the direct voltage component which occurs in said strength control circuit is separated from the constant potential by a second separating means (9, C2, C3) of direct voltage and the charge state of said second separating means of direct voltage is controlled by a second control signal (DCN2) for controlling the direct voltage component occurring in the control circuit.
4. A method according to any of the previous claims, **characterized** in that said first and second control signals are switched to an active state at least part of them at the same time.
5. A method according to any of the previous claims, **characterized** in that said first and second control signals are switched to an active state before the start of the time slot which contains information of the received signal.
6. A method according to any of the previous claims, **characterized** in that for reducing of the offset voltage, to the output (P2) of said separating

means a second signal (Vref, s62) is connected which is formed on the basis of the first signal (s61) preceding said separating means.

7. A circuit arrangement for processing the received signal, which  
5 comprises a demodulator (2) for demodulating the received radio frequency signal into a baseband, a control circuit (5) for controlling the strength of the baseband signal, first separating means (6, C1) for separating of direct voltage occurring in the baseband signal and for converting the A/D converter signal into a digital form, **characterized** in that the circuit  
10 arrangement comprises means (10) for controlling the direct voltage component of the first baseband signal preceding said separating means on the basis of the first control signal (DCN1) and means (11) for controlling the direct voltage component of the second baseband signal following the separating means on the basis of the second control signal (DCN2) which  
15 second control signal may be identical to said first control signal.

8. A circuit arrangement according to claim 7, **characterized** in that it comprises a second separating means (9, C2, C3) for separating the direct voltage component which occurs in said control circuit from the constant  
20 potential.

9. A circuit arrangement according to claims 7 or 8, **characterized** in that it comprises means for controlling the charge state of said second separating means (C2, C3) by said second control signal for controlling the  
25 direct voltage component which occurs in the control circuit.

10. A circuit arrangement according to any of the previous claims 7-9, **characterized** in that the signal line between the demodulator (2) and the first separating means (6, C1) has been to direct voltage coupled.  
30

11. A circuit arrangement according to any of the previous claims 7-10, **characterized** in that the demodulator (2) is an I/Q demodulator and to the output of its quadrature signal, the first branch (3a) has been connected for processing a baseband quadrature signal and to the output of the in-phase signal, the second branch (3b) has been connected for processing the in-  
35 phase baseband signal.

13.

12. A circuit arrangement according to any of the previous claims 7-11, **characterized** in that it comprises means (63) for connecting the second signal (Vref, s62) to the output (P62) of the separating means (C61) and means (64, 65) for forming said second signal (s62) on the basis of the first signal (s61) preceding the separating means (C61).
13. Use of a method according to any of the previous claims 1-6 or a circuit arrangement according to any of the previous claims 7-12 in a direct conversion receiver.
14. Use of a method according to any of the previous claims 1-6 or a circuit arrangement according to any of the previous claims 7-12 in a receiver of a mobile station.
15. Use of a method according to any of the previous claims 1-6 or a circuit arrangement according to any of the previous claims 7-12 in a digital, time-division mobile communication system.

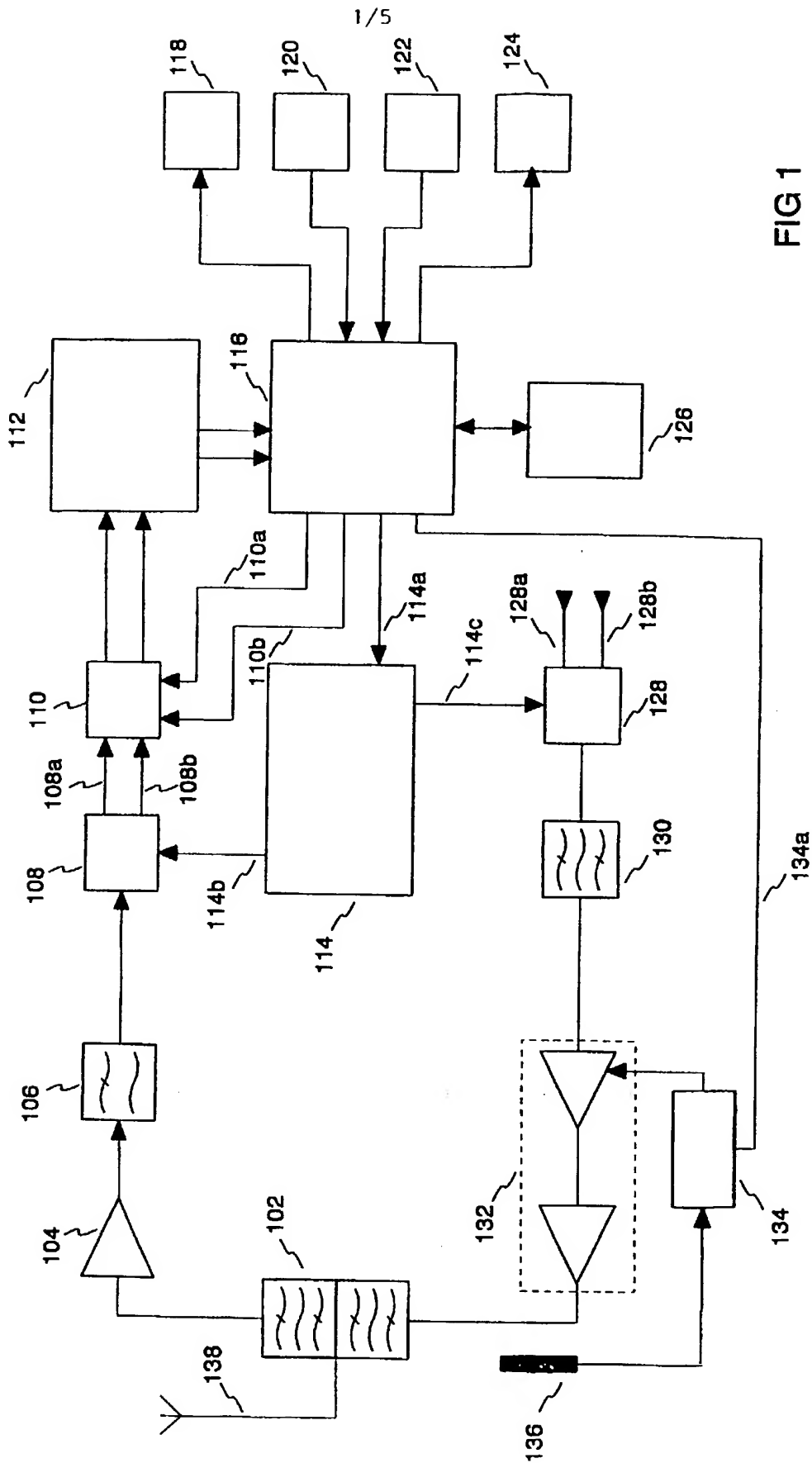


FIG 1

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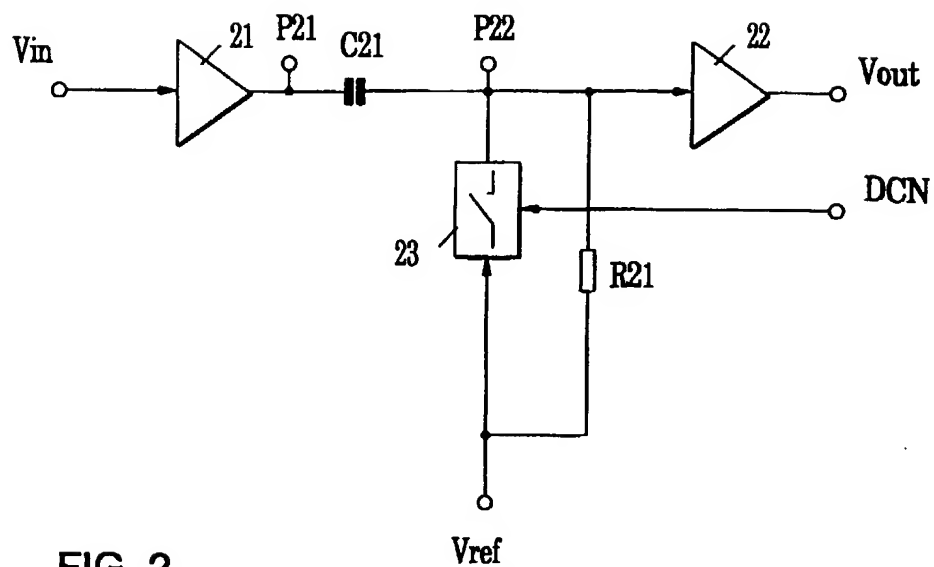


FIG. 2

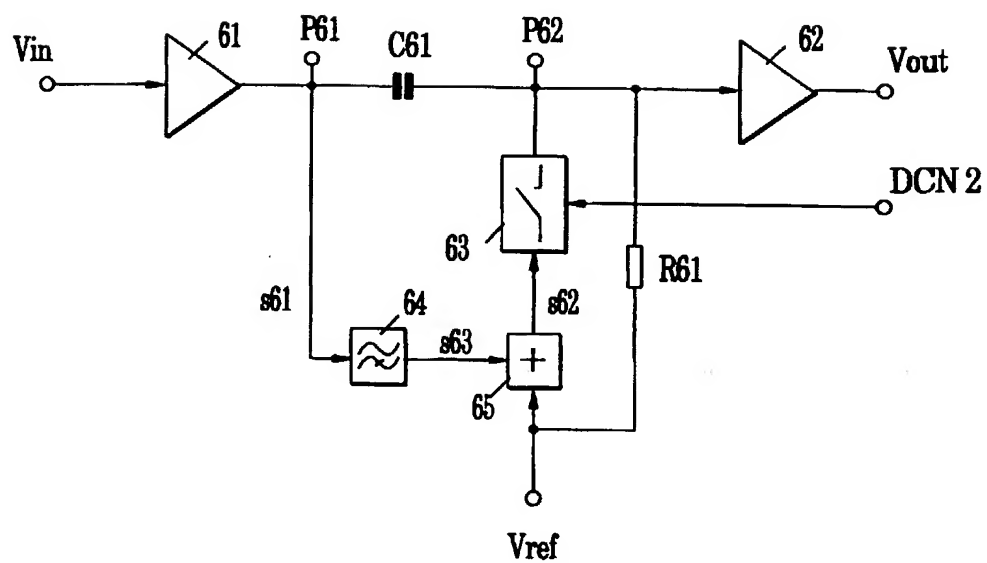


FIG. 6

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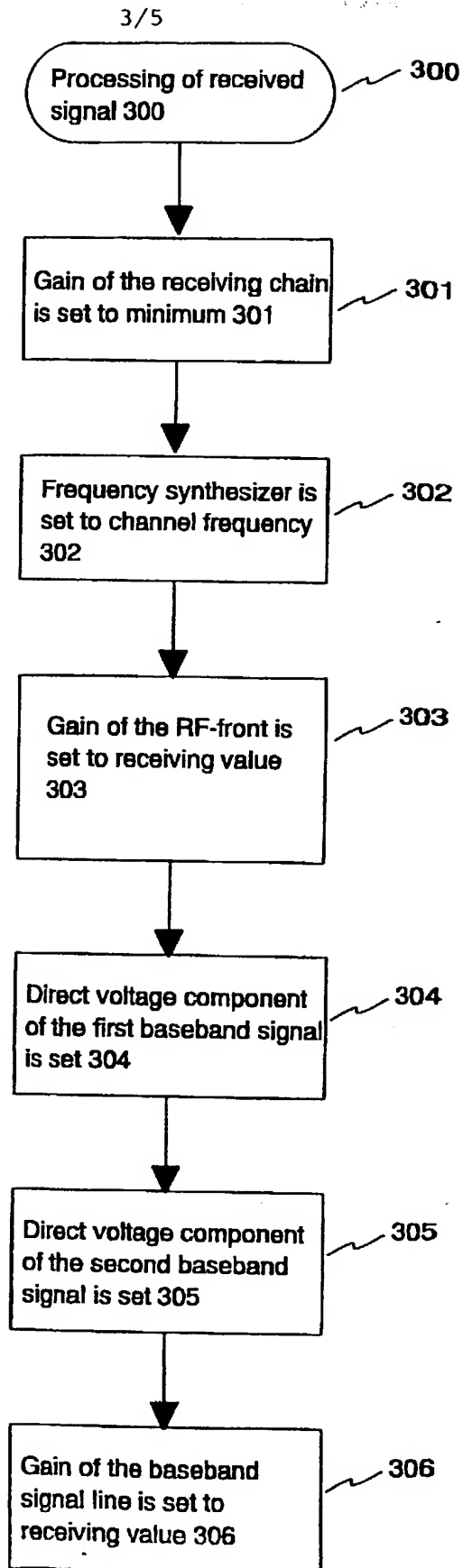


FIG. 3

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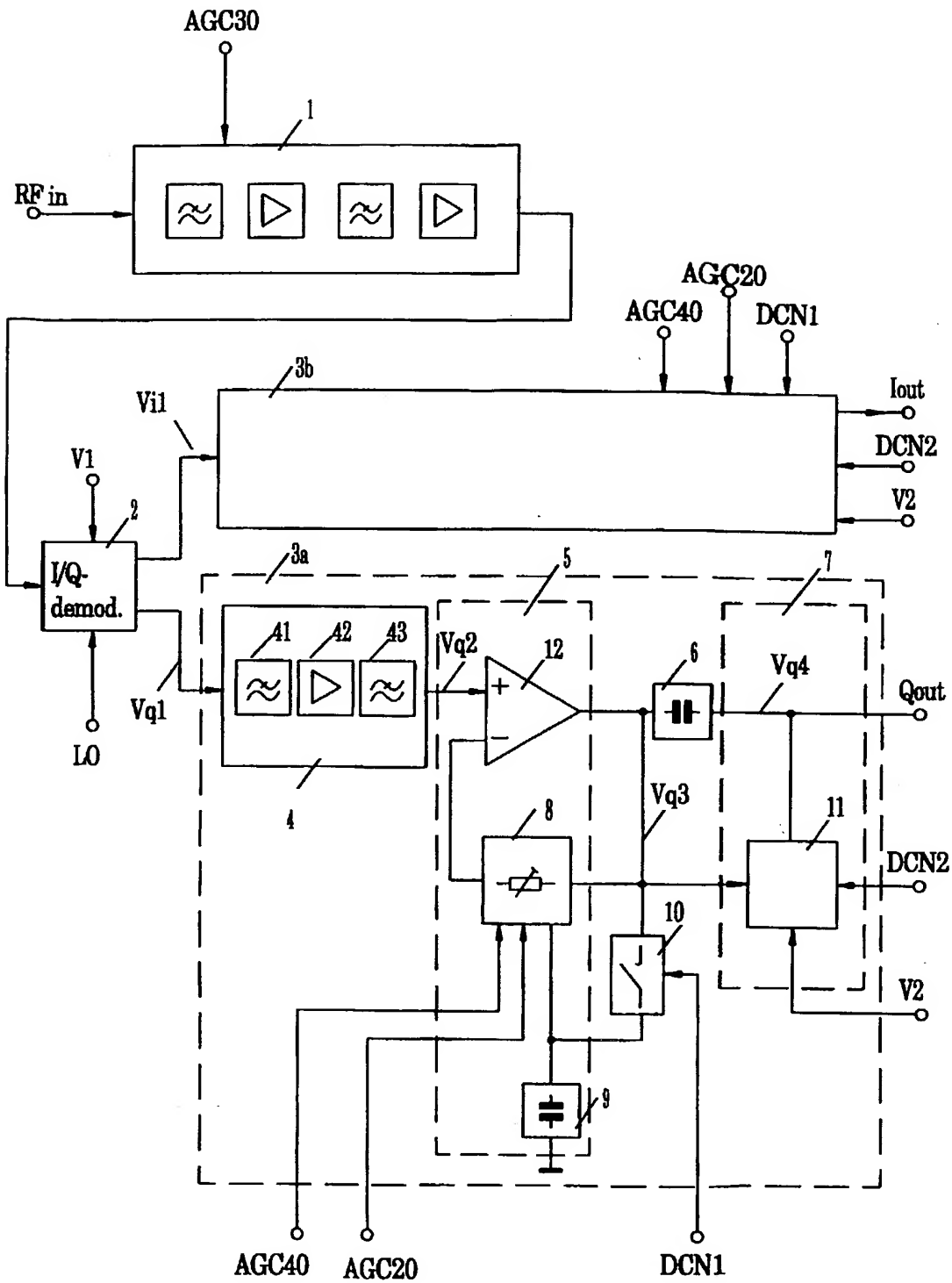


FIG. 4

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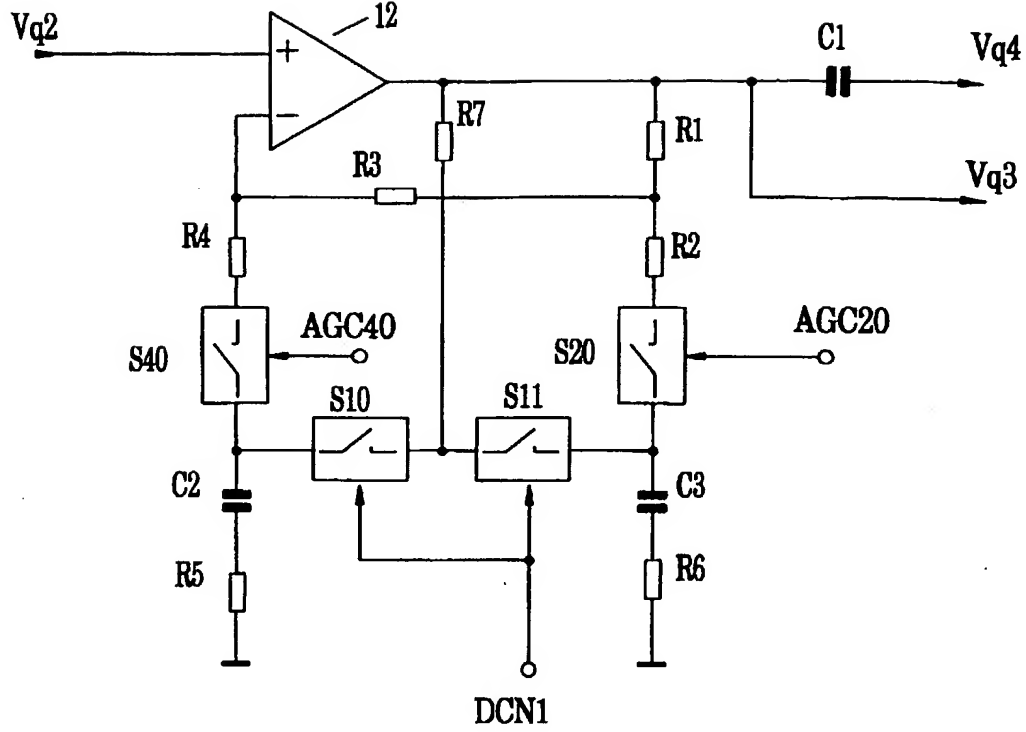


FIG. 5

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## INTERNATIONAL SEARCH REPORT

International application No.

PCT/FI 97/00073

## A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04B 1/12

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

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## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5461340 A (CHAHABADI ET AL), 24 October 1995 (24.10.95), column 1, line 19 - column 2, line 39, claim 1 ---	1-15
X	US 5212826 A (RABE ET AL), 18 May 1993 (18.05.93), column 4, line 9 - line 40, claim 1 --	1-15
A	US 5359652 A (MULDER ET AL), 25 October 1994 (25.10.94), column 1, line 32; column 2, line 62 --	1-15
A	US 4745594 A (TAKAHASHI), 17 May 1988 (17.05.88), abstract -----	1-15

☐ Further documents are listed in the continuation of Box C.☒ See patent family annex.

## \* Special categories of cited documents:

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"&amp;" document member of the same patent family

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

01/07/97

International application No.

PCT/FI 97/00073

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